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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,415	10/23/2003	David W. Boerstler	AUS920030369US1	8491
45327	7590	08/10/2005	EXAMINER	
IBM CORPORATION (CS) C/O CARR LLP 670 FOUNDERS SQUARE 900 JACKSON STREET DALLAS, TX 75202			LEJA, RONALD W	
			ART UNIT	PAPER NUMBER
			2836	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/692,415

**Applicant(s)**

BOERSTLER ET AL.

**Examiner**

Ronald W. Leja

**Art Unit**

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 31 May 2005.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-4, 7-12, 29, 31 and 32 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-4, 7-12, 29, 31 and 32 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 23 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

Art Unit: 2836

Claims 8, 9, 11 and 12 are objected to because of the following informalities: In Claims 8 and 9, in line 1, "the voltage" should read as "a voltage". In Claim 11, line 1, "System" should be "system" for consistency purposes. In Claim 12, line 2, "fuse blow" should be deleted. Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-4, 7-12, 29, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. (6,141,245) in view of Aipperspach et al. (6,509,236).

Bertin et al. disclose in Figure 1, a system for de-coupling a capacitive path (30) from an IO pad (25) and a protected component (20) (a processor for Claims 2 & 32) wherein a first circuit (50) is a fuse (for Claim 3) and a second circuit (55) (fuse blow pad for Claim 4) able to cause the first circuit to cease conducting in response to variations in voltage or current wherein a node is coupled to the first circuit (between

Art Unit: 2836

(55) and (30)) and a capacitive path (30) is decoupled from the IO pad and protected component (20) in response to the first circuit (50) ceasing to conduct. (See Col. 4, lines 19-44). Bertin et al. do not appear to disclose details about the protective device (30) except that it is commonly known in the art (see Col. 4, lines 27-31). However, Aipperspach et al. teach that commonly known protective devices are diodes, i.e. (212 & 214). It would have been obvious to use the known diodes of Aipperspach et al. as the commonly known protective device of Bertin et al. as a means to protect the protected component from both positive and negative transients arriving at the IO pad, before the device was mounted in a pcb or system, and therefore, less susceptible to ESD events, thus resulting in a more reliable product. As far as Claims 10 and 32, Bertin et al. disclose that a certain current flow is used to blow the fuse(s) (50), but do not exactly disclose the application of voltages to the pads and at values less than for activation of the protective device(s). It is the opinion of the Examiner, that it would have been obvious to apply different voltages at the respective pads as a means to effectively get a current to flow from one voltage potential to another voltage potential, which would blow the fuse, thereby resulting in the desired de-coupling of capacitance, which is undesirable as processor speeds increase (see Col. 1, lines 12-26). It also would have been obvious to keep the voltage potentials to a level insufficient to activate the protective device(s) since activation of the protective device would render the fuse blowing process unreliable, due to the different current flow path, (i.e. from the fuse blow pad thru the appropriate diode and not the IO pad). Claims 11 and 12 essentially add that the second circuit further requires a control input and that a single signal can control multiple second circuits. Figure 2(a) of Bertin et al. show the use of second circuit having control inputs (80a-n) and

Art Unit: 2836

controlled by a signal (92), but do not specifically disclose that the second circuit shorts to ground upon receipt of the signal, but rather merely connects the fuse to a power supply. It is the opinion of the Examiner, that it would have been obvious to apply the appropriate voltage to the appropriate pad so as to get the desired current flow thru the fuse for blowing of the fuse. Use of a power supply would be necessary in either case, since if the fuse blow pad is ground, a voltage would be necessary at the IO pad so as to get the current flow. Claim 29 requires the use of a laser for fuse blowing. Aipperspach et al. teach the use of a laser for fuse blowing. It would have been obvious to implement the laser as a means for fuse blowing so as to avoid having to apply a voltage source to each IO pad needing its associated fuse blown, thereby easing the process especially if a large number of fuses needed to be selectively blown.

Applicant's arguments filed 5/31/2005 have been fully considered but the amendment of 5/31/2005 necessitated the new grounds of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date

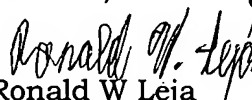
Art Unit: 2836

of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald W. Leja whose telephone number is (571)272-2053. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Ronald W Leja  
Primary Examiner  
Art Unit 2836

rwl  
August 4, 2005

